REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1, 4, 6, 9, 10 and 21 are active in this application, Claims 1, 4 and 6 having been amended, Claims 2, 3 5, 7 and 8 canceled, and new Claim 21 added by the present Amendment, Claims 11-20 having been withdrawn from consideration as directed to a non-elected invention.

In the outstanding Official Action Claims 1-10 were rejected under 35 USC §102(b) as being anticipated by Ikeda et al (US Patent 6,403,421); and Claims 1-4 and 6-10 were rejected under 35 USC §102(b) as being anticipated by Aritome (US Patent 5,949,101).

In light of the outstanding grounds for rejection, Claim 1 has been amended to clarify the structure of the claimed semiconductor device. Support for the changes to Claim 1 is found in the original claims, including the claims canceled by the present amendment, and no new matter has been added.

Also submitted herewith is new Claim 21 which further defines the depression formed in the isolation insulating film as including a tapered U-shaped portion, consistent with the depiction of the depression 34 shown in Figure 5 and as illustrated, albeit unnumbered, in Figure 2A, and consistent with the Plasma CVD formation method disclosed at page 12, lines 7-19 of the specification. Accordingly, no new matter has been added by the submission of new Claim 21.

Applicants respectfully submit that amended Claim 1 patentably defines over the cited Ikeda et al patent, for the reasons next discussed.

In particular, amended Claim 1 recites that "each of the first and second side surfaces of the first and second floating gates is entirely opposed to the control gate line".

On the other hand, in the Ikeda et al. device, it is evident from FIG. 11I that only a portion of a side surface of each floating gate 33 is opposed to a control gate line 31. Therefore, Ikeda et al. does not disclose or obviate this feature of the structure recited in amended Claim 1.

Furthermore, amended Claim 1 also recites, "the first side surface of the first floating gate entirely aligning with a side surface included in the first element-formation region and defined by the isolation trench, and the second side surface of the second floating gate entirely aligning with a side surface included in the second element-formation region and defined by the isolation trench." In other words, with the claimed structure, the first side surface of the first floating gate entirely aligns with an interface between the first element-formation region and the isolation insulating film formed in the isolation trench. This is also true with the second side surface of the second floating gate.

On the other hand, according to Ikeda et al., a portion of the floating gate 33 is formed on an upper surface (top surface) of an isolation insulating film 24a (refer to FIG. 11I), such that in the Ikeda et al. device, a side surface of the floating gate 33 is not entirely aligned with the interface between the element-formation region and the isolation insulating film 24a. Therefore, Ikeda et al. does not disclose or obviate this further feature of the structure recited in amended Claim 1.

In view of the deficiencies identified in Ikeda et al., it is respectfully submitted that Ikeda et al. clearly does not anticipate the presently claimed invention and that the pending active Claims 1, 4, 6, 9, 10 and 21 patentably define over Ikeda et al.

Moreover, amended Claim 1 further recites, "an isolation insulating film which is formed at least in the isolation trench and which includes a depression formed in an upper surface thereof and an uppermost portion located higher than a surface of the semiconductor substrate and lower than the upper surface of each of the first and second floating gates."

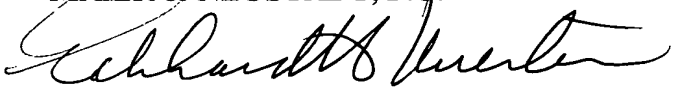
Accordingly, in the claimed invention, the uppermost portion of the isolation insulating film is located higher than the surface of the semiconductor substrate.

On the other hand, according to Aritome, it is evident from FIG. 9E that the uppermost portion of the isolation insulating film 2 is located lower than the surface of the semiconductor substrate 1B. Therefore, Aritome does not disclose this feature stated in amended Claim 1. Accordingly, in view of this deficiency, it is respectfully submitted that Aritome clearly does not anticipate the presently claimed invention and that the pending active Claims 1, 4, 6, 9, 10 and 21 likewise patentably define over Aritome.

Consequently, in view of the present amendment, no further issues are believed to be outstanding, and the present application is believed to be in condition for formal allowance. An early and favorable action to that effect is respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)
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